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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,297	WALTER ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because they do not have sufficiently descriptive labels. Blank boxes in drawings should be labeled descriptively unless it is a well-known component.

Claim Objections

2. In claim 3, line 3, to avoid problems of antecedent basis, "the scaling unit" should be ---the analog scaling unit---.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-8, 10, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 is considered to be vague and indefinite because it contains the confusing recitation, "wherein at least one active integrator, the analog scaling unit is an analog arithmetic circuit to which as the at least one analog setting value, a DC voltage signal or a direct current signal is delivered." In this recitation, it is unclear to one having ordinary skill in the art as to what "wherein at least one active integrator" refers and how the "at least one active integrator" is part of the analog scaling unit.

Claims 3-8, 10, and 17 are rejected under 35 U.S.C. 112, second paragraph, because they incorporate the lack of clarity present in parent claim 2.

Claim 3 is further rejected under 35 U.S.C. 112, second paragraph, because it includes the recitation, "as the actuator" with no previous mention of any actuator.

Claim 17 is further rejected under 35 U.S.C. 112, second paragraph, because it recites, "wherein at least one active integrator, as the actuator for at least one direct current signal and the active integrator, is connected to the processor circuit and to the analog scaling unit." It is unclear, however, to one having ordinary skill in the art how "at least one active integrator" can be "the actuator for . . . the active integrator".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,207,101 to Haynes.

Haynes discloses a two-wire ultrasonic transmitter comprising a sensor that detects a quantity to be measured (column 2, lines 19-22), an analog end stage, comprising an amplifier circuit, connected downstream of the sensor (Figure 4b, "52"), a processor circuit, including a processor and drive circuit (column 7, lines 41-42) and an analog measurement signal transmission path (see subsequent circuitry from X1 in Figure 4a), the analog end stage converting an output of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured (column 2, lines 26-29 and column 8, lines 6-36), the electronic transducer controlled/programmed with the processor circuit (column 2, lines 21-25), wherein during the normal operation of the ultrasonic transmitter apparatus, the processor circuit is shifted temporarily into a sleep mode (column 9, lines 44-47, column 14, lines 51-58, and column 17, lines 12-15), the analog measurement signal path and an analog scaling unit (i.e. current control circuit) are used, the output signal of the sensor and at least one analog setting value is supplied to the analog scaling unit (column 6, lines 1-3 and column 4, lines 57-60), and the output of the analog scaling unit is supplied to the analog end stage to maintain the output in the range of 4mA to 20mA (see Figures 2 and 4b and column 16, lines 54-56).

Haynes also discloses that the analog scaling unit is an analog arithmetic power supply circuit that implements a power source that produces a non-zero DC voltage signal as the analog setting value (column 4, lines 60-61).

Haynes also discloses that the analog end stage includes, between the analog scaling unit and the subsequent analog end stage circuitry, and attenuator

comprising an RC element (column 2, lines 58-60 and column 8, lines 52-64) wherein an error output of the attenuator can be compensate by a control circuit (i.e. comparator with threshold detection) (column 8, line 65 to column 9, line 9).

7. Claims 1, 2, 9, and 16, as may best be understood, are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,480,131 to Roper et al.

Roper discloses an electrical transducer using a two-wire process (column 1, lines 6-14) comprising an analog sensor that detects a quantity to be measured (column 4, lines 19-23), an analog end stage which is connected downstream of the sensor that converts an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured (column 4, lines 26-29), a processor circuit, wherein the processor circuit is not connected serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized (column 4, lines 26-29), the electronic transducer being controlled by the processor circuit (column 4, lines 33-51) wherein during normal operation of the electrical transducer, the processor circuit is shifted temporarily into a low-power sleep mode (abstract and column 3, lines 23-30), the analog measurement signal transmission path includes an analog scaling unit (i.e. an analog arithmetic circuit) the output of the sensor and at least one analog setting value, in the form of a DC voltage signal, are supplied to the analog scaling unit, and the output signal of the analog scaling unit is supplied to the analog end stage (column 6, lines 50-64 and Figure 3).

Roper also discloses a power source that produces a non-zero output current (column 4, lines 52-55).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of U.S. Patent No. 5,207,101 to Haynes.

As noted above, the invention of Roper teaches many of the features of the claimed invention and while Roper does disclose an analog scaling unit and an analog end stage, Roper does not specifically include a connected attenuator.

Haynes discloses a two-wire ultrasonic transmitter comprising a sensor that detects a quantity to be measured (column 2, lines 19-22), an analog end stage, comprising an amplifier circuit, connected downstream of the sensor (Figure 4b, "52"), a processor circuit, including a processor and drive circuit (column 7, lines 41-42) and an analog measurement signal transmission path (see subsequent circuitry from X1 in Figure 4a), the analog end stage converting an output of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured (column 2, lines 26-29 and column 8, lines 6-36), the electronic transducer controlled/programmed with the processor circuit (column 2, lines 21-25),

wherein during the normal operation of the ultrasonic transmitter apparatus, the processor circuit is shifted temporarily into a sleep mode (column 9, lines 44-47, column 14, lines 51-58, and column 17, lines 12-15), the analog measurement signal path and an analog scaling unit (i.e. current control circuit) are used, the output signal of the sensor and at least one analog setting value is supplied to the analog scaling unit (column 6, lines 1-3 and column 4, lines 57-60), and the output of the analog scaling unit is supplied to the analog end stage to maintain the output in the range of 4mA to 20mA (see Figures 2 and 4b and column 16, lines 54-56).

Haynes also discloses that the analog scaling unit is an analog arithmetic power supply circuit that implements a power source that produces a non-zero DC voltage signal as the analog setting value (column 4, lines 60-61).

Haynes also discloses that the analog end stage includes, between the analog scaling unit and the subsequent analog end stage circuitry, an attenuator comprising an RC element (column 2, lines 58-60 and column 8, lines 52-64), having an adjustable time constant (i.e. adjustable resistor and capacitor values) wherein an error output of the attenuator can be compensate by a control circuit (i.e. comparator with threshold detection) (column 8, line 65 to column 9, line 9).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper to include a connected attenuator, as taught by Haynes, because, as suggested by Haynes, the combination would have improved the performance of the process control transmitter of Roper by effectively minimizing dead band (column 8, lines 52-64).

10. Claims 3, 4, and 17, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of U.S. Patent No. 5,886,565 to Yasui et al.

As noted above, the invention of Roper teaches many of the features of the claimed invention including a DC reference voltage connected to the analog scaling unit and processor circuit, but does not specify how this reference voltage is supplied.

Yasui teaches a reference voltage generating circuit having an integrator that generates a reference voltage using a voltage dividing circuit that divides a voltage supplied from a power source for use by the integrator (abstract).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper to include an active integrator for generating the reference voltage, as taught by Yasui because Yasui suggests a corresponding circuit applicable and needed in the invention of Roper in order to generate a reference voltage as well as assuring low power consumption and a stable output characteristic (column 1, lines 44-47).

Although the combination of Roper and Yasui provides an active integrator electrically coupled to the processing circuit rather that part of the processing circuit itself, it would have been obvious to one having ordinary skill in the art to provide the integrator and the processing circuit as one circuit in order to adhere to space constraints as well as allow greater control by controlling the reference voltage as

needed using internal circuitry of the processor. Further, it has been held that forming in one piece which has formerly been formed in two pieces and put together involves only routine skill in the art (see Howard v. Detroit Stove Works, 150 U.S. 164 (1893)).

11. Claims 5 and 7, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of U.S. Patent No. 6,057,794 to Takamuki.

As noted above, the invention of Roper teaches many of the features of the claimed invention and while the invention of Roper does include an analog scaling unit as an arithmetic circuit, Roper does not specify that the analog scaling unit comprise an analog multiplier, adder, and subtractor.

Takamuki teaches a sigma-delta modulation circuit including an analog multiplier, adder, and subtractor (column 10, lines 5-14) with an adder connected through a delay circuit and a converter to the input of a multiplier and an adder and subtractor connected to the output of the multiplier (Figure 5).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper to specify that the analog scaling unit comprise an analog multiplier, adder, and subtractor, as taught by Takamuki, because Roper includes a sigma-delta circuit as part of the analog scaling unit and Takamuki suggests a corresponding circuit applicable and necessary to implement the sigma-delta circuit using a small, simple configuration (column 2, lines 25-27).

12. Claims 6 and 10, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of Takamuki and further in view of U.S. Patent No. 5,714,903 to Bruccoleri et al.

As noted above, the invention of Roper and Takamuki teaches many of the features of the claimed invention and while the combination does teach an analog scaling unit including an analog multiplier, the combination does not specify that the multiplier be a single-quadrant multiplier.

Bruccoleri teaches a low-consumption analog multiplier that is a single-quadrant multiplier (column 4, line 66 to column 5, line 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper and Takamuki to specify that the multiplier by a single-quadrant multiplier, as taught by Bruccoleri, because Bruccoleri suggests a corresponding multiplier for use in the invention of Roper and Takamuki using a multiplier that would have improved efficiency by lowering current consumption while increasing error compensation (column 4, line 66 to column 5, line 3).

13. Claim 8, as may best be understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of Takamuki and further in view of U.S. Patent No. 5,420,379 to Zank et al.

As noted above, the invention of Roper and Takamuki teaches many of the features of the claimed invention including an analog scaling unit, but does not specifically include a plurality of transistors and a plurality of operational amplifiers.

Zank teaches an electromagnetic position transducer including analog and/or digital integrators implemented using a plurality of transistors and operational amplifiers (column 29, line 66 to column 30, line 4).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper and Takamuki to include a plurality of transistors and a plurality of operational amplifiers, because the invention of Roper and Takamuki does include an integrator in the analog scaling unit and Zank suggests that integrators are commonly implemented using a plurality of transistors and operational amplifiers and therefore the combination would have provided a conventional means for implementing the integrators of Roper and Takamuki (column 29, line 66 to column 30, line 4).

14. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roper in view of U.S. Patent No. 5,252,967 to Brennan et al.

As noted above, the invention of Roper teaches many of the features of the claimed invention and while the invention of Roper teaches operation in two-wire mode, Roper does not disclose means for operation in three-wire mode.

Brennan teaches a reader/programmer for two and three wire utility data communications systems including three power supply terminals (i.e. receptacles) (column 6, lines 18-25) wherein upon automatic detection of a predetermined voltage of an interrogation signal at the terminals (column 7, lines 43-55 and column 9, lines 47-49), the measurement device sends a wake-up signal to its

microprocessor (column 10, lines 30-37) and based upon the interrogation signal, which powers the device (column 9, lines 26-31), operates in either two or three wire mode (column 9, line 50 to column 10, line 10).

It would have been obvious to one having ordinary skill in the art to modify the invention of Roper to include means for operation in three-wire mode, as taught by Brennan, because Roper teaches a transmitter for use in pressure and/or flow measurement and, as suggested by Brennan, the combination would have provided means for a utility meter, such as a pressure or flow meter, to be used in two or three wire modes thereby increasing the versatility of the device while reducing the burden on the user (column 2, lines 7-32).

Response to Arguments

15. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

It is noted, however, that Applicant argues, "[i]n contrast to the electrical transducer defined by amended claim 1, in this known ultrasonic transmitter, the processor circuit is connected serially between the transducer and the end stage. Therefore an analog measurement signal transmission path as required by amended claim 1 is **not** realized."

The Examiner asserts that while independent claim 1 as been amended to specify that the processor is not connected serially between the transducer and the end stage, such an amendment has not been made to independent claim 16.

It is also noted that while Applicant has modified the drawings Figure 1 still contains blank boxes as do Figures 2, 3, 6a, 6b, and 7.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 5,956,663 to Eryurek teaches a signal processing technique which separates signal components in a sensor for sensor diagnostics.

U.S. Patent No. 5,416,723 to Zyl teaches a loop powered process control transmitter.

U.S. Patent No. 5,083,091 to Frick et al. teaches a charge balanced feedback measurement circuit.

JP Patent Application Publication No. 04-359399 to Tamura et al. teaches a three-wire signal processor that converts a three-wire signal into a two-wire signal.

U.S. Patent No. 3,948,098 to Richardson et al. teaches a vortex flow meter transmitter that can be used in two-wire or three-wire operation.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
September 19, 2004

MARC S. HOFF
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